

REMARKS

Claims 1, 3-5, and 7-16 are pending. By this amendment, claims 2 and 6 are canceled, claims 1 and 12-15 are amended, and new claim 16 is added.

The Office Action rejects claims 1-14 under the judicially created doctrine of obviousness type double patenting over claims 1-14 of related applications 10/614,859, 10/614,860, 10/614,861, 10/614,862 and 10/614,864. It is submitted that this rejection for each of these applications should be provisional, until one of the applications is otherwise ready to issue. That application should then be allowed to issue, and the double patenting rejection, if still in affect, should be made non-provisional, and applicants will then consider whether to submit a terminal disclaimer.

The Office Action rejects claims 1-15 under 35 USC 103 over O'Brien (US Pat. 5,247,638) in view of Totani (US Pat. 5,175,842). This rejection is respectfully traversed.

The storage system of the present invention includes one or more first path coupling said channel unit to a first cache unit of said plurality of cache units, one or more second path coupling said channel unit to a second cache unit of said plurality of cache units and not being in common with said first path, one or more third path coupling said control unit to said first cache unit, and one or more fourth path coupling said control unit to said second cache unit and not being in common with said third path. Accordingly, the "transfer of data between the channel unit and first cache units", the "transfer of data between the channel unit and second cache units", the "transfer of data between the control unit and first cache units", and the "transfer of data between the control unit and second cache units" can be executed in parallel. So, the process of reading/writing data related to the host computer from/to the first cache unit, the process of reading/writing data related to the host computer from/to the second cache unit, the process of reading/writing data between the first cache unit and the disk device, and the process of reading/writing data between the second cache unit and the disk device can be executed efficiently.

In contrast, O'Brien does not disclose the plurality of cache memories. Thus, O'Brien does not disclose the plurality of paths of the present invention connecting the plurality of cache memories and the channel unit or the control unit. As a result, O'Brien cannot attain the results of the present invention.

Further, Totani discloses memory control unit 2 is disposed among the host computer 1, the plurality of caches 8, 9 and the external memory unit 3 to transfer the data. However, if it is assumed that the memory control unit 2 corresponds to the claimed channel unit, Totani does not disclose the relation of the claimed invention among the control unit, the plurality of cache memories, and the plurality of paths.

Similarly, if it is assumed that the memory control unit 2 corresponds to the claimed control unit, Totani does not disclose the relation among the channel unit, the plurality of cache memories and the plurality of paths. Accordingly, Totani cannot attain the effects of the claimed invention.

If O'Brien and Totani are combined as suggested, Totani discloses only the structure corresponding to one of the channel unit and the control unit. Thus, it is unclear which of the whether the relation of the caches 8, 9 and the memory control unit 2 of Totani would correspond to the channel unit or the control unit, but there is no disclosure that it would correspond to both. Further, the applied references provide no motivation for the asserted combination.

Further, if it is assumed that the multipath storage director 110 of O'Brien corresponds to the memory control unit 2 of Totani, O'Brien does not disclose or provide motivation of the concept of the relation among the control unit, the plurality of cache memories and the plurality of paths as claimed in the present invention. O'Brien does not disclose structure corresponding to the plurality of cache memories and the control unit.

In addition, even if it is assumed that the cluster control 111 of O'Brien corresponds to the memory control unit 2 of Totani, O'Brien does not disclose, and provides no motivation for the claimed relation among the control unit, the plurality of cache memories, and the plurality of paths. O'Brien does not disclose structure corresponding to the plurality of cache memories and the channel unit.

Moreover, even if it is assumed that the disk drive manager 102 of O'Brien corresponds to the memory control unit 2 of Totani, O'Brien does not disclose, and provides no motivation for the claimed relation among the channel unit, the plurality of cache memories, and the plurality of paths. O'Brien does not disclose structure corresponding to the plurality of cache memories and the channel unit.

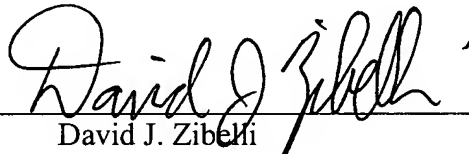
Accordingly, even if combined, the resulting combination would not render obvious the claimed invention. Further, the applied references provide no motivation for the asserted combination.

For at least the above reasons, it is submitted that claim 1, and all dependent claims, would not have been obvious over the applied references. Withdrawal of the rejection is requested. Claim 16 is allowable for the same reasons.

For these reasons, it is submitted that the application is in condition for allowance. Consideration and allowance in due course are solicited.

The Office is authorized to charge any additional fees under 37 C.F.R. § 1.16, § 1.16, or § 1.36, or credit of any overpayment to Kenyon & Kenyon Deposit Account No. 11-0600.

Respectfully submitted,



David J. Zibelli
Registration No. 36,394

Date: March 16, 2005

KENYON & KENYON
1500 K Street, N.W. - Suite 700
Washington, D.C. 20005-1257
Tel: (202) 220-4200
Fax: (202) 220-4201
548775_DC01